UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,815	12/01/2003	Philip George Emma	YOR920030544US1 (163-22)	5561

24336 7590 06/13/2007	EXAMINER	
KEUSEY, TUTUNJIAN & BITETTO, P.C. 20 CROSSWAYS PARK NORTH SUITE 210 WOODBURY, NY 11797	MCLEAN MAYO, KIMBERLY N	
	ART UNIT	PAPER NUMBER
	2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/724,815	EMMA ET AL.
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- **The MAILING DATE of this communication appears on the cover sheet with the correspondence address** --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>04 April 2007</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-10 and 12-48</u> is/are pending in the application.

　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) <u>1-10,12 and 36-48</u> is/are allowed.

6) ☒ Claim(s) <u>13-30 ands 33-35</u> is/are rejected.

7) ☒ Claim(s) <u>31 and 32</u> is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　a) ☐ All　b) ☐ Some *　c) ☐ None of:

　　1. ☐ Certified copies of the priority documents have been received.

　　2. ☐ Certified copies of the priority documents have been received in Application No. _____.

　　3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
　Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
　Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   The enclosed detailed action is in response to the Amendment submitted on April 4,

2007.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless —
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 13-16, 21-27, 30 and 33-35 are rejected under 35 U.S.C. 102(b) as being

anticipated by Pomerene et al. (USPN: 4,679,141).

Regarding claims 13-14, 22, 24 and 30, Pomerene discloses a cache (Figure 19, Reference 101);

a meta-structure hierarchically arranged on accordance with size and speed such that faster and

more accurate prefetching is provided by coaction of hierarchical meta-structures (Figure 19,

Reference 131; C 11, L 32-37, L 58-64; Figure 19, Backup area; C 11, L 25-32; C 19, L 6-36; C

16, L 57-60, L 16-68; C 17, entire; more accurate prefetching [of predicted target addresses] is

accomplished by storing predicted target addresses for branches the processor issuing or will

use); a meta-collector (Figure 19, self loading controls, analyzer and stager) which collects and

records [in the backup area of the PBHT] temporally and spatially sequential unique meta-

information entries (branch address and predicted target address) related to access of entries of a

meta-structure (C 16, L 9-16; PBHT; entries in the PBHT are accessed when the branch has been

executed by the processor), each corresponding to a cache line to enable hierarchical meta-

structure operation to provide prefetching of the meta-information entries to a fastest meta-structure level based upon look ahead context information (C 16, entire, C 17, entire, C 18, entire, C 19, L 1-36).

Regarding claim 15, Pomerene discloses a predicted branch table for identifying a sequence of predicted taken branches that a processor will soon encounter (C 8, L 49-50; C 11, L 58-64; table is comprised of the all the predicted target addresses in the PBHT).

Regarding claim 16, Pomerene discloses the meta-information is correlated to program flow in a processor (the meta-information is branch prediction information which is correlated to the flow of branch instruction in a program and thus is correlated to program flow in a processor).

Regarding claim 21, Pomerene discloses a plurality of memory storage structures arranged to prefetch information for stages of a circuit (the PBHT prefetches information via the meta-collector from the backup BHT for stages of the branch processing done using the processor and the cache).

Regarding claim 23, Pomerene discloses the prefetching step including associating cache lines with information addresses in the meta-collector (C 17, L 32-68; C 18, entire; C 19, L 1-35; branch addresses accessed in the cache which are being analyzed by the meta-collector [analyzer/stager])

Regarding claim 25, Pomerene discloses identifying a sequence of predicted taken branches that

a processor will soon encounter by employing a predicted branch table (C 8, L 49-50; C 11, L

58-64; table is comprised of the all the predicted target addresses in the PBHT).

Regarding claim 26, Pomerene discloses correlating the meta-information to program flow in the

processor (the meta-information is branch prediction information which is correlated to the flow

of branch instruction in a program and thus is correlated to program flow in a processor).

Regarding claim 27, Pomerene discloses evicting cache line information from the meta-collector

when a corresponding cache line is replaced (inherent, when information is removed/evicted

from the meta-structures the information is no longer available for the meta-collector when

processing the segment entries to perform prefetching).

Regarding claims 33-34, Pomerene discloses updating meta-information between levels of the

hierarchical meta-structure (C 19, L 65-68).

Regarding claim 35, Pomerene disclose (C 12, L 4-8; C 13, L 8-24).

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 17-20 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Pomerene (USPN: 4,679,141) in view of Zuraski (USPN: 7,024,545).

Regarding claims 17-19, Pomerene discloses the limitations cited above in claims 7 and 13

respectively, however, Pomerene does not explicitly disclose storing the meta-structures in a

hierarchically arranged cache including a first level cache and a second level cache. Zuraski

discloses storing a meta-structure in a hierarchically arranged cache including a first level cache

and a second level cache (C 12, L 61+; C 28, L 57-58; C 14, L 7+; C 12, L 64+; C 28, L 59-60).

Pomerene indicates that the PHBT resembles a cache in many ways (C 11, L 38-57) and thus it is

evident from one of ordinary skill in the art would consider using a cache since a cache includes

faster memory structure. Hence, it would have been obvious to one of ordinary skill in the art to

store Pomerene's meta-structure in a hierarchically arranged cache for the desirable purpose of

faster system performance.

Regarding claim 20, Pomerene discloses the unique meta-information including at least one of a

branch address and a predicted target address for information to be prefetched [from the backup

BHT](C 8, L 49-50; C 16, L 51-60).

Regarding claim 28, Pomerene discloses the limitation cited above for claim 22, however,

Pomerene does not disclose storing evicted information to a next level memory in a cache

hierarchy. Zuraski discloses storing evicted information to a next level memory in a cache

hierarchy (abstract). In Pomerene's system all the data stored in the lower level memory is also

stored in the higher level memory and thus when data is evicted there is no need to store the data in the higher level memory. This feature causes the higher level memory to be extremely slow and large. The feature taught by Zuraski provides a fast and efficient method of operating hierarchical memories using smaller hierarchical memories. Hence, it would have been obvious to one of ordinary skill in the art to incorporate Zuraski's teachings with the system taught by Pomerene for the desirable purpose of efficiency and improved performance.

Regarding claim 29, Pomerene discloses the limitations cited above for claim 22, however, Pomerene does not disclose writing to a next level memory area in a cache hierarchy a cache miss address. It is well known in the art to write to a L2 cache to the location, which caused a miss in the L1 cache when using hierarchical caches. This feature provides improved performance by carrying out the memory operation using the cache memories in oppose to writing to main memory. Hence, it would have been obvious to one of ordinary skill in the art to use hierarchical caches in Pomerene's system such that a cache miss address is written to a higher level cache when a cache miss occurs in the lower level cache for the desirable purpose of improved performance.

Response to Arguments

6.   Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Regarding Applicant's arguments with respect to claim 13, the Examiner disagrees. Claim 13

does not state "look ahead context information. The claim calls for storing spatial and temporal

meta-information related to access of entries of a meta-structure.

Regarding Applicant's arguments with respect to claim 22, the Examiner disagrees. Claim 22

does not state collecting and recording a sequence of entries in a meta-structure corresponding to

a cache line. The claim calls for storing spatial and temporal meta-information related to access

of entries of a meta-structure.

Allowable Subject Matter

7.   Claims 1-10, 12 and 36-48 are allowed.

8.   Claims 31-32 are objected to as being dependent upon a rejected base claim, but would

be allowable if rewritten in independent form including all of the limitations of the base claim

and any intervening claims.

Conclusion

9.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Monday-Friday (10-6:30).
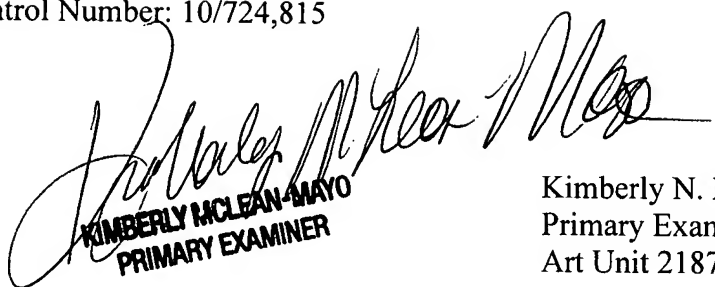
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kimberly N. McLean-Mayo
Primary Examiner
Art Unit 2187

KNM

June 9, 2007